

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62706BN, TB62706BF

16BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

The TB62706BN, TB62706BF is specifically designed for LED and LED DISPLAY constant current drivers.

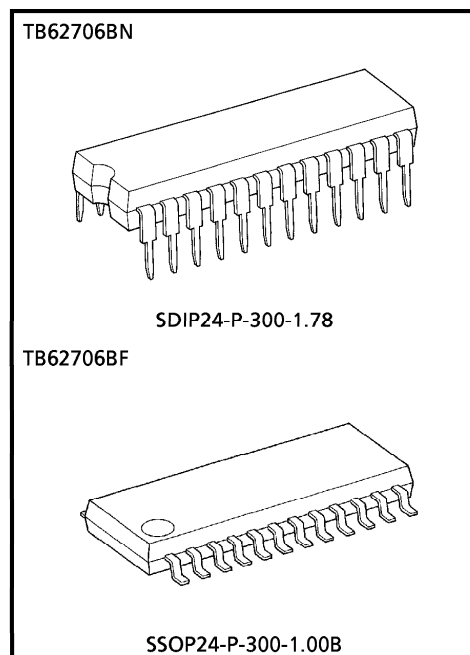
This constant current output circuits is able to set up external resistor ($I_{OUT} = 5\sim 90\text{mA}$). (Note)

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 16bit shift register, latch, AND-GATE and Constant Current Drivers.

FEATURES

- Constant Current Output : Can set up all output current with one resister for 5 to 90mA.
- Maximum Clock Frequency : $f_{CLK} = 15$ (MHz) (Cascade Connected Operate, $T_{opr} = 25^{\circ}\text{C}$)
- 5V C-MOS Compatible Input
- Package : SDIP24-P-300-1.78~1.778mmPitch~ (TB62706BN)
SSOP24-P-300-1.00B~1.0mmPitch~ (TB62706BF)
- Constant Output Current Matchong :



Weight
 SDIP24-P-300-1.78 : 1.22g (Typ.)
 SSOP24-P-300-1.00B : 0.32g (Typ.)

OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
$\geq 0.4\text{V}$	$\pm 6.0\%$	5~40mA
$\geq 0.7\text{V}$	$\pm 6.0\%$	5~90mA

(Note)

(Note) TB62706BF can be used under limited P_D !
 $(P_D \leq 1.04\text{W, with PCB})$

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TERMINAL DIScription

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register.
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$ -terminal, and hold data with "L" level input.
5~20	$\overline{\text{OUT0}}\sim\overline{7}$	Output terminals.
21	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~15) do off with "H" level input of $\overline{\text{ENABLE}}$ -terminal, and do on with "L" level input.
22	SERIAL-OUT	Output terminal of a serial-data for next SERIAL-IN terminal.
23	R-EXT	Input terminal of connects with a resistor for to set up all output current.
24	V_{DD}	5V Supply voltage terminal.

TRUTH TABLE

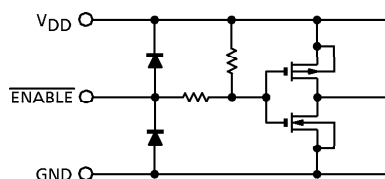
CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	OUT0 ... OUT5 ... OUT7	SERIAL-OUT
UP	H	L	D_n	$D_n \dots D_{n-7} \dots D_{n-15}$	D_{n-15}
UP	L	L	D_{n+1}	No change	D_{n-14}
UP	H	L	D_{n+2}	$D_{n+2} \dots D_{n-5} \dots D_{n-13}$	D_{n-13}
DOWN	X	L	D_{n+3}	$D_{n+2} \dots D_{n-5} \dots D_{n-13}$	D_{n-13}
DOWN	X	H	D_{n+3}	Off	D_{n-13}

(Note) $\text{OUT0}\sim\text{15} = \text{on}$ in case of $D_n = \text{H}$ level and $\text{OUT0}\sim\text{15} = \text{off}$ in case of $D_n = \text{L}$ level.

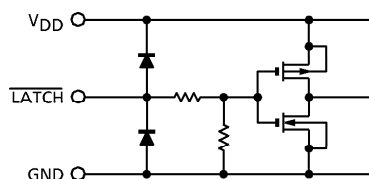
A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

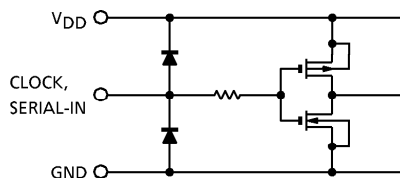
1. $\overline{\text{ENABLE}}$ terminal



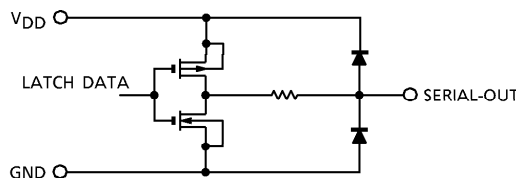
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	0~7.0	V
Input Voltage	V _{IN}	-0.4~V _{DD} + 0.4	V
Output Current	I _{OUT}	90	mA
Output Voltage	V _{OUT}	-0.5~17.0	V
Clock Frequency	f _{CK}	15	MHz
GND Terminal Current	I _{GND}	1440	mA
Power Dissipation	P _D	1.78 (BN-type : ON PCB, Ta = 25°C)	W
		1.00 (BF-type : ON PCB, Ta = 25°C)	
Thermal Resistance	R _{th(j-a)}	BN : 70 (BN-type : ON PCB)	°C/W
		BF : 120 (BF-type : ON PCB)	
Operating Temperature	T _{opr}	-40~85	°C
Storage Temperature	T _{stg}	-55~150	°C

(Note) BN-type : Ambient temperature delated above 25°C in the proportion of 14.2mW/°C

BF-type : Ambient temperature delated above 25°C in the proportion of 8.3mW/°C

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V
Output Voltage	V _{OUT}	—	—	—	15.0	V
Output Current	I _O	OUTn, DC 1 circuit	5	—	88	mA
	I _{OH}	SERIAL-OUT	—	—	1.0	
	I _{OL}	SERIAL-OUT	—	—	-1.0	
Input Voltage	V _{IH}	—	0.7 V _{DD}	—	V _{DD} + 0.3	V
	V _{IL}	—	-0.3	—	0.3 V _{DD}	
LATCH Pulse Width	t _w LAT	V _{DD} = 4.5~5.5V	100	—	—	ns
CLOCK Pulse Width	t _w CLK		50	—	—	ns
ENABLE Pulse Width	t _w EN		4500	—	—	ns
Set-Up Time for DATA	t _{setup} (D)		60	—	—	ns
Hold Time for DATA	t _{hold} (D)		20	—	—	ns
Set-Up Time for LATCH	t _{setup} (L)		100	—	—	ns
Hold Time for ENABLE	t _{hold} (L)		60	—	—	ns
Clock Frequency	f _{CLK}		Cascade operation	—	—	10.0
Power Dissipation	P _D	Ta = 85°C (BN-type)	—	—	0.92	W
		Ta = 85°C (BF-type)	—	—	0.50	

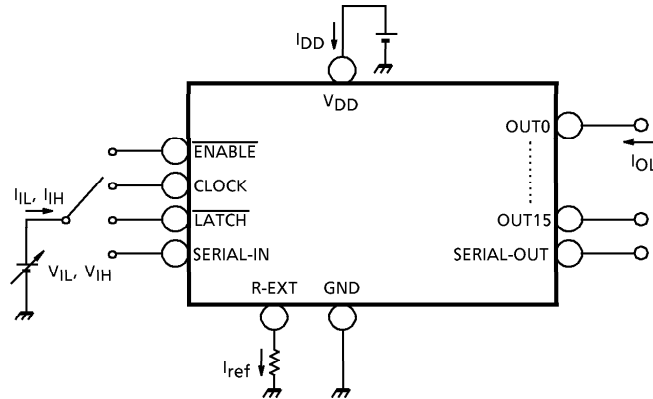
ELECTRICAL CHARACTERISTICS ($V_{DD} = 5.0V$, $T_a = 25^\circ C$ unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT	
Input Voltage	"H" Level	V_{IH}	—	$T_a = -40 \sim 85^\circ C$	0.7 V_{DD}	—	V_{DD}	V	
	"L" Level	V_{IL}	—	$T_a = -40 \sim 85^\circ C$	GND	—	0.3 V_{DD}		
Output Leakage Current		I_{OH}	—	$V_{OH} = 15.0V$	—	—	10	μA	
Output Voltage	SERIAL-OUT	V_{OL}	—	$I_{OL} = 1.0mA$	—	—	0.4	V	
		V_{OH}	—	$I_{OH} = -1.0mA$	4.6	—	—		
Output Current 1		I_{OL1}	—	$V_{CE} = 0.7V$	34.1	40.0	45.9	mA	
		I_{OL2}	—	$V_{CE} = 0.4V$					$R_{EXT} = 470\Omega$ (Include current matching)
Current Skew		ΔI_{OL1}	—	$I_O = 40mA$, $V_{CE} = 0.4V$	$R_{EXT} = 470\Omega$	—	± 1.5	± 6.0	%
Output Current 2		I_{OL3}	—	$V_{CE} = 0.7V$	64.2	75.5	86.8	mA	
		I_{OL4}	—	$V_{CE} = 0.4V$					$R_{EXT} = 250\Omega$ (Include current matching)
Current Skew		ΔI_{OL2}	—	$I_O = 75mA$, $V_{CE} = 0.7V$	$R_{EXT} = 250\Omega$	—	± 1.5	± 6.0	%
Supply Voltage Regulation		$\% / V_{DD}$	—	$R_{EXT} = 470\Omega$, $T_a = -40 \sim 85^\circ C$	—	1.5	5.0	$\% / V$	
Pull-Up Resistor		$R_{IN (up)}$	—	—	150	300	600	Ω	
Pull-Down Resistor		$R_{IN (down)}$	—	—	100	200	400	Ω	
Supply Current	"OFF"	$I_{DD (off) 1}$	—	$R_{EXT} = OPEN$, $OUT1 \sim 8 = off$	—	0.6	1.2	mA	
		$I_{DD (off) 2}$	—	$R_{EXT} = 470\Omega$, $OUT1 \sim 8 = off$	3.5	5.8	8.0		
		$I_{DD (off) 3}$	—	$R_{EXT} = 250\Omega$, $OUT1 \sim 8 = off$	6.5	10.7	15.0		
	"ON"	$I_{DD (on) 1}$	—	$R_{EXT} = 470\Omega$, $OUT1 \sim 8 = on$	10.0	16.0	22.0		
		$I_{DD (on) 2}$	—	$R_{EXT} = 250\Omega$, $OUT1 \sim 8 = on$	18.0	28.3	38.5		

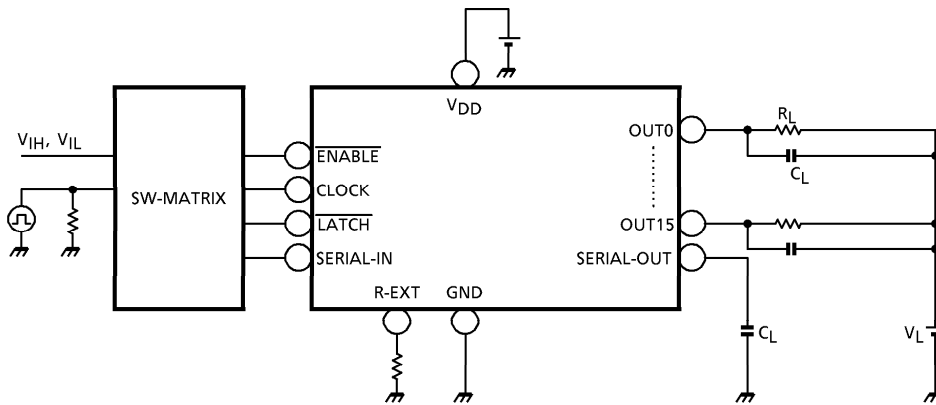
SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	CLK-OUTn	t _{pLH}	—	V _{DD} = 5.0V V _{CE} = 0.4V V _{IH} = V _{DD} V _{IL} = GND R _{EXT} = 470Ω V _L = 3.0V R _L = 65Ω C _L = 10.5pF	—	1200	1500	ns
	LATCH-OUTn				—	1200	1500	
	ENABLE-OUTn				—	1200	1500	
	CLK-SOUT				—	30	70	
Propagation Delay Time ("H" to "L")	CLK-OUTn	t _{pHL}	—		—	700	1000	ns
	LATCH-OUTn				—	700	1000	
	ENABLE-OUTn				—	700	1000	
	CLK-SOUT				—	30	70	
Pulse Width	CLK	t _w CLK, CLK	—		—	20	30	ns
	LATCH	t _w LAT, LAT	—		—	10	25	ns
Set-up Time for LATCH	L-H	t _{setup} (L)	—		—	25	50	ns
	H-L	t _{setup} (C)	—		—	25	50	ns
Hold Time for LATCH	L-H	t _{hold} (L)	—		—	0	15	ns
	H-L	t _{hold} (C)	—		—	0	15	ns
Maximum CLOCK Rise Time	t _r	—	—		—	—	10	μs
Maximum CLOCK Fall Time	t _f	—	—		—	—	10	μs
Output Rise Time	t _{or}	—	—	150	300	600	ns	
Output Fall Time	t _{of}	—	—	150	300	600	ns	

TEST CIRCUIT
DC characteristic



AC characteristic

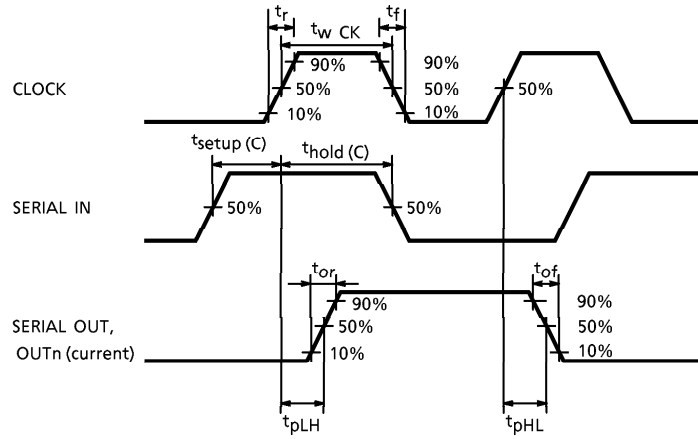


PRECAUTIONS for USING

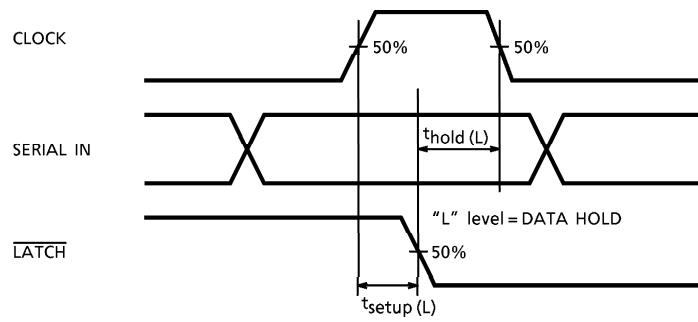
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

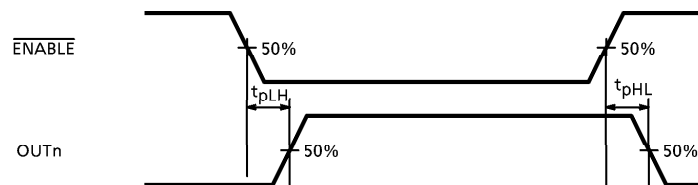
1. CLOCK-SERIAL OUT, OUTn

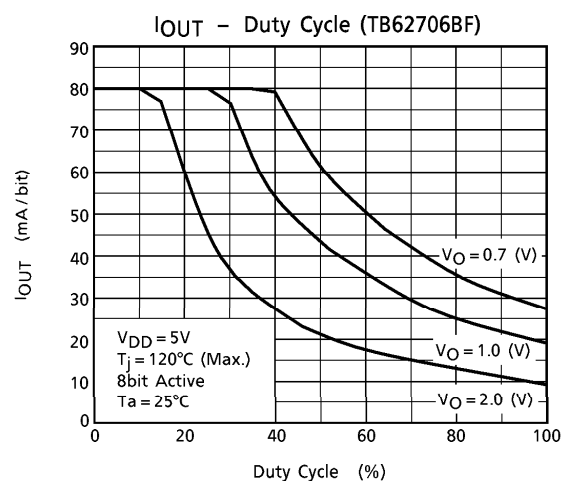
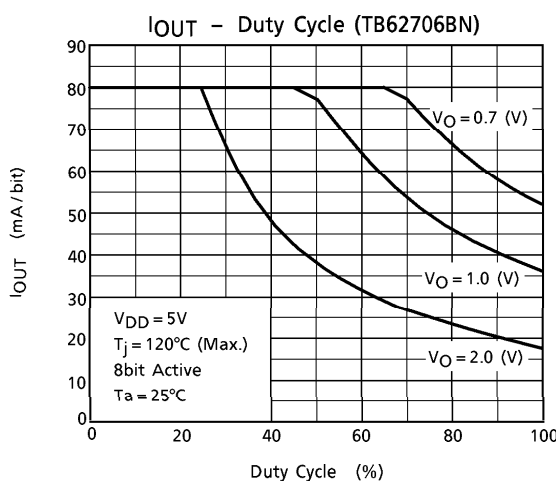
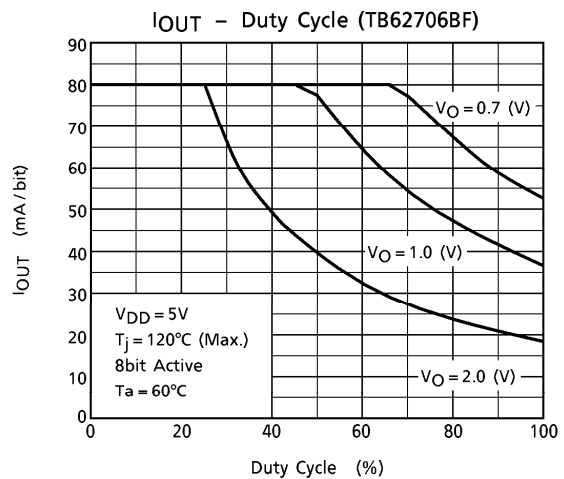
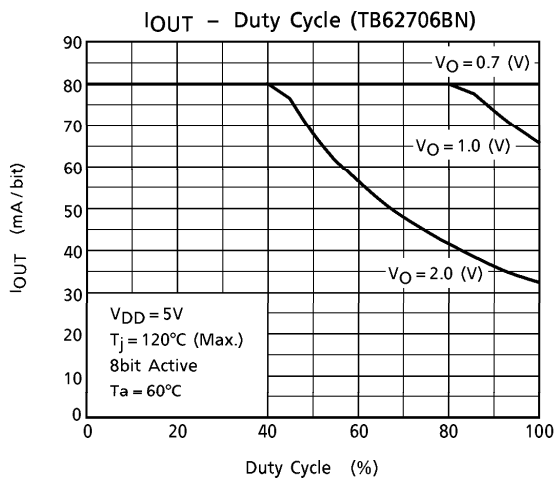
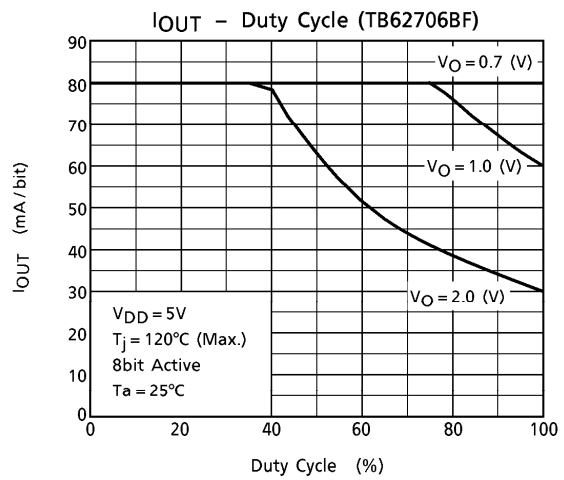
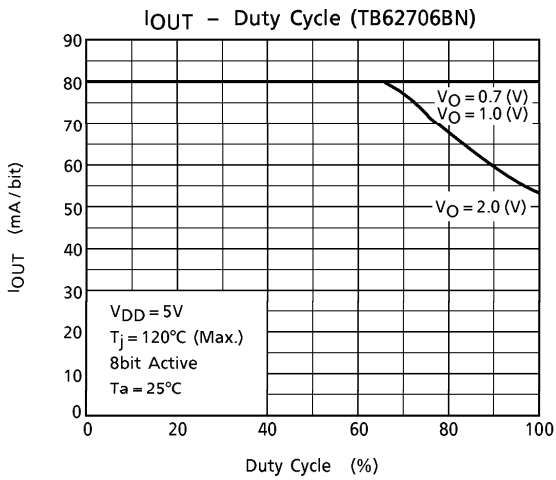


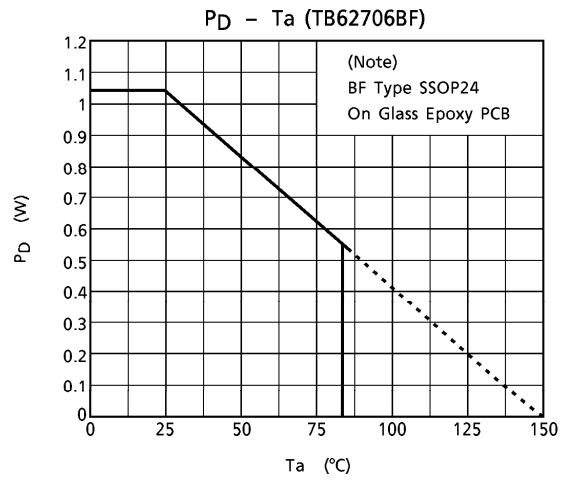
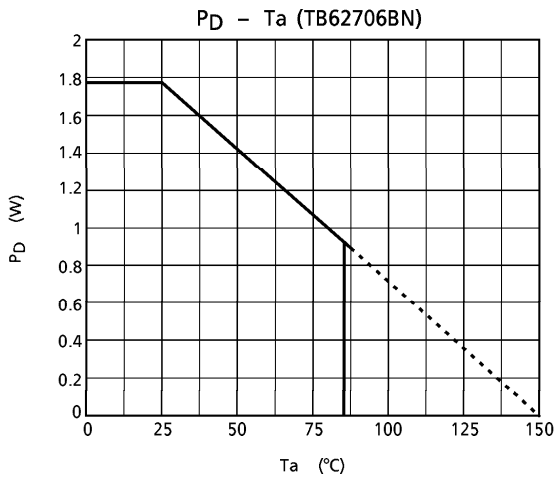
2. CLOCK-LATCH



3. ENABLE-OUTn







LED DRIVER TB6270X SERIES APPLICATION NOTE

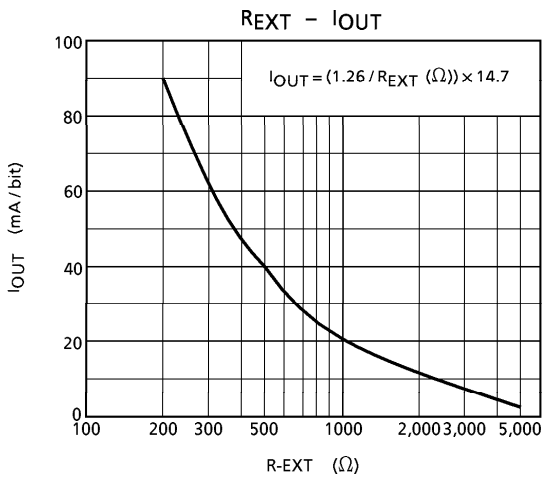


Fig. 1

[1] Output current (I_{OUT})

I_{OUT} is set by the external resistor (R-EXT) as shown in Fig.1.

[2] Total supply voltage (V_{LED})

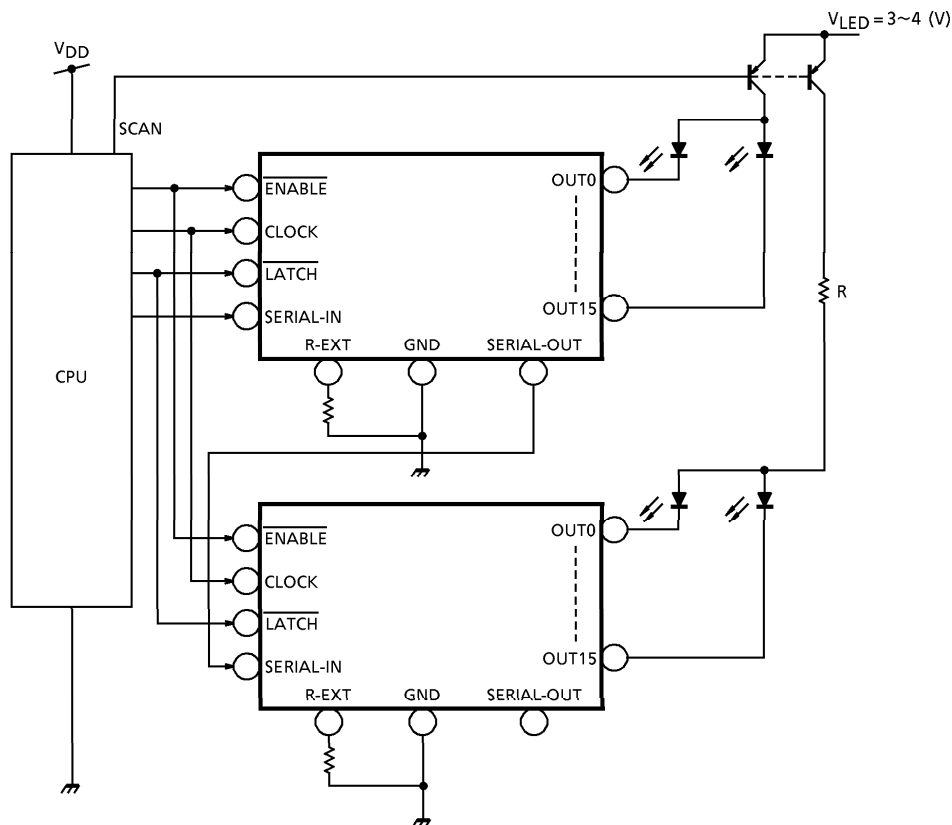
This device can operate 0.4~0.7V (V_O).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

$$V_{LED} \text{ (total supply voltage)} = V_{CE} (T_r V_{sat}) + V_f \text{ (LED Forward voltage)} + V_O \text{ (I}_C \text{ supply voltage)}$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage (V_O).



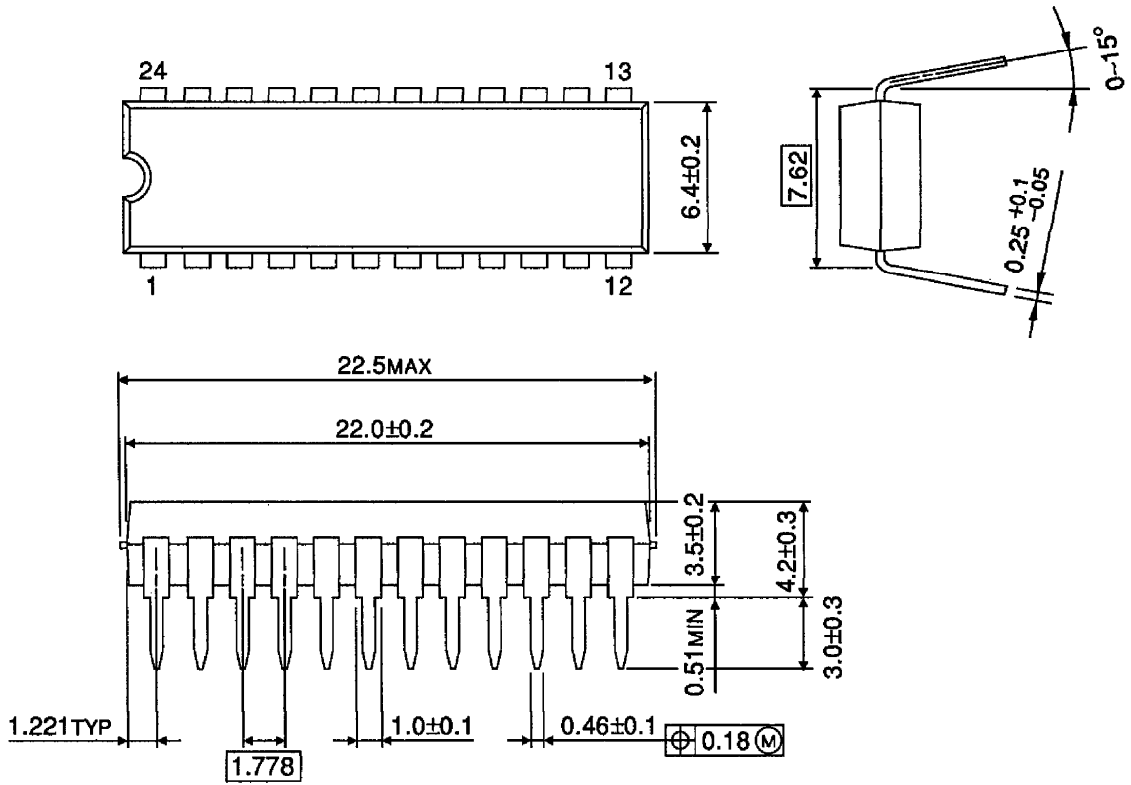
[3] Pattern layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss-operate. So we would like you to pay attention to pattern layout to minimize inductance.

OUTLINE DRAWING
SDIP24-P-300-1.78

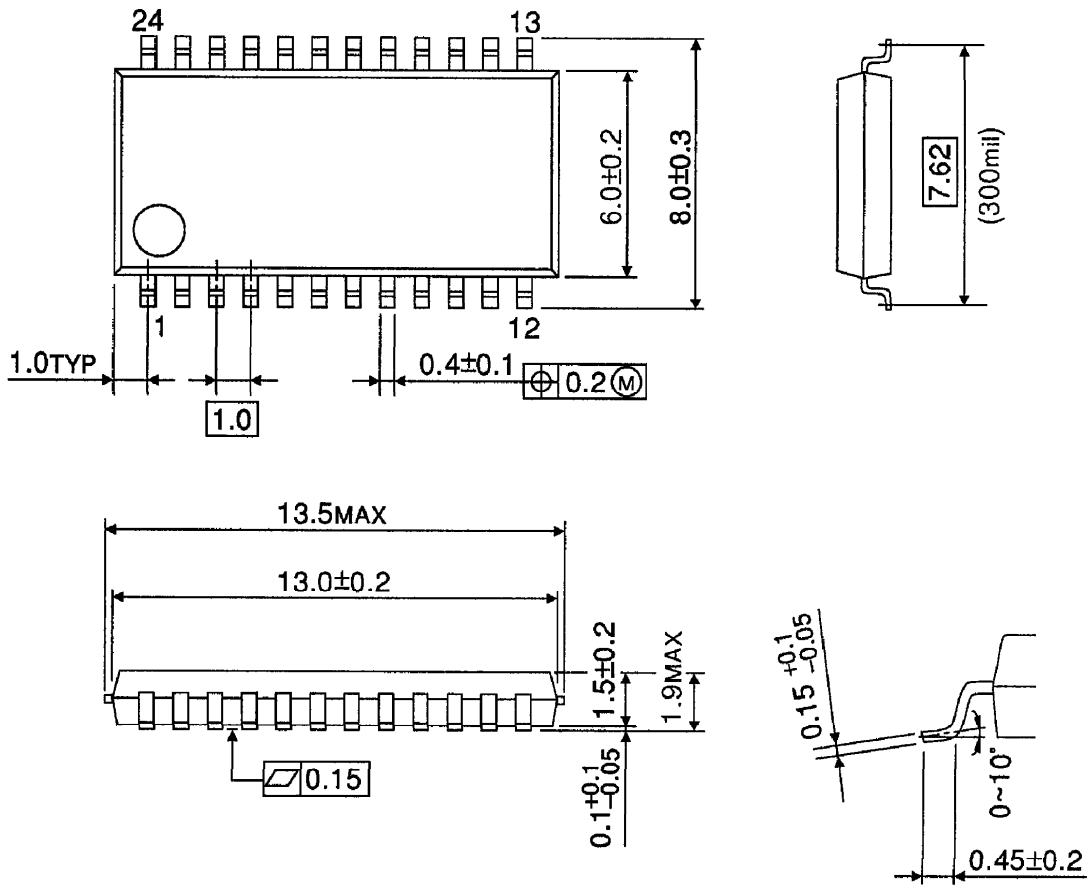
Unit : mm



Weight : 1.22g (Typ.)

OUTLINE DRAWING
SSOP24-P-300-1.00B

Unit : mm



Weight : 0.32g (Typ.)